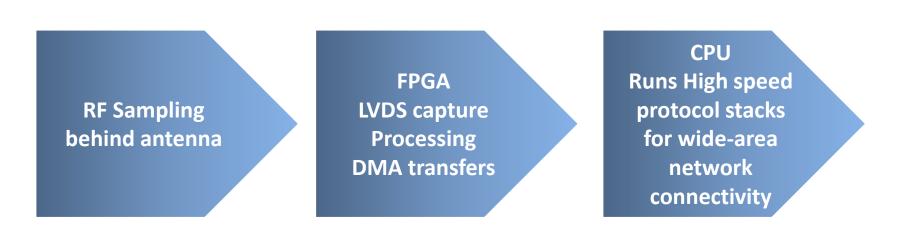


Embedded Tech Trends 2014

New EW architectures based on tight coupling of FPGA and CPU processing





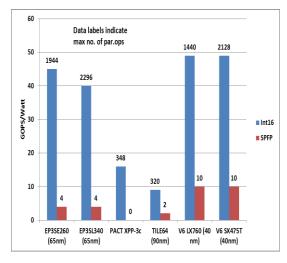
Low Phase Noise Clocking Multi-Channel Synchronization

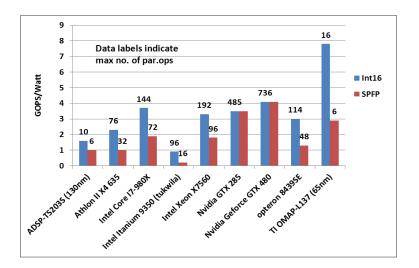
Low Power Parallel Processing Very high-speed Transceivers

High-end processors Wide-band on the backplane Multi-Root Complex Communication



Parallel Processing and Power consumption





Configurable logic devices



A study financed by the National Science Foundation (Alan George, Herman Lam, and Greg Stitt - IEEE magazine Computing in Science and Engineering - Jan/Feb 2011)

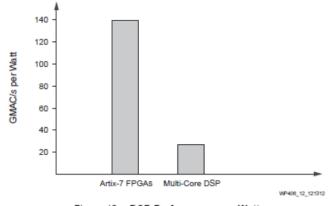
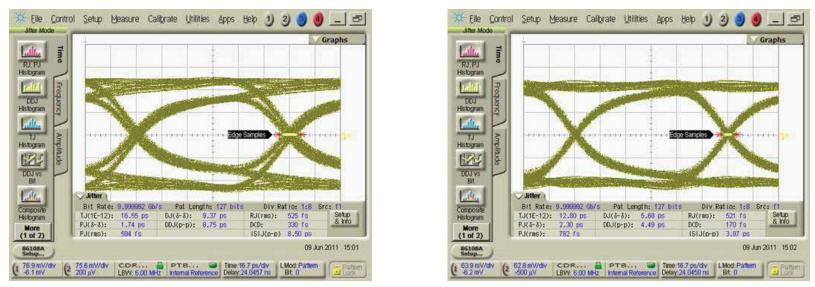


Figure 12: DSP Performance per Watt

http://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf

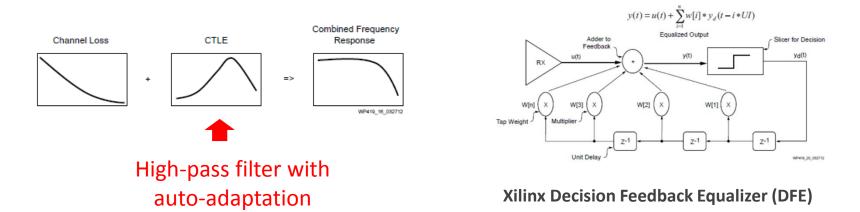


RX-TX techniques for FPGA Transceivers



GTX Tranceiver 10 Gb/s Eye Diagram without (left) and with 2 dB post tap de-empahsis (right)

Peak to peak ISI jitter reduced by more than two

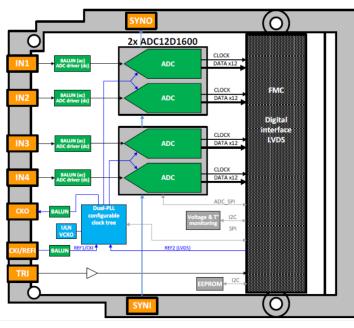




RF Sampling ADC & VITA 57 ADC FMC

Benefits of RF-Sampling

- A single direct RF-sampling ADC can replace an entire IF-sampling or ZIF-sampling subsystem of mixers, LO synthesizers, amplifiers, filters, and ADCs
- Reduction of bill of materials (BOM) cost, design time, board size, weight, and power.
- Analog frequency down-conversion function moved into the DSP, FPGA, or ASIC, where frequencies and bandwidths can be controlled digitally, enabling maximum system flexibility and re-configurability
- Example 4 channels at 1300 Msps 12 bit (1300 Mhz on the LVDS
- to Virtex-7)



Example of RF Sampling ADC FMC







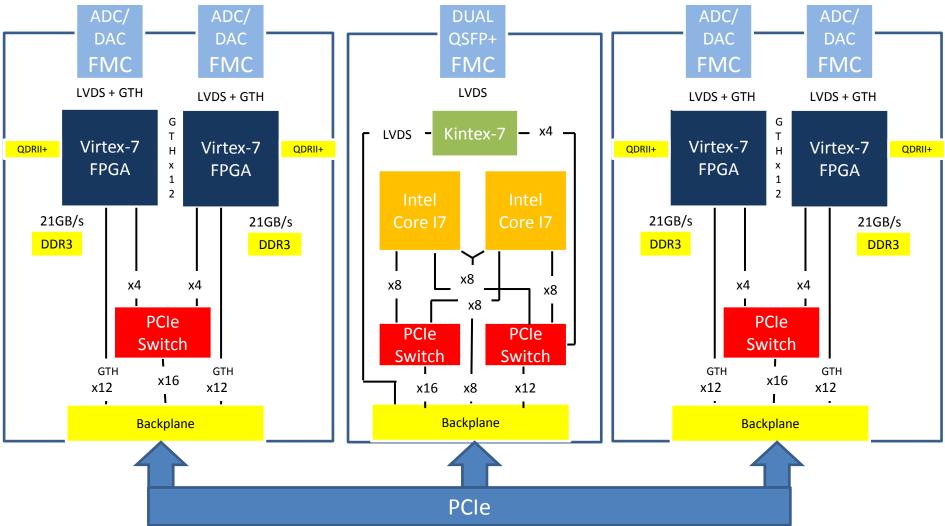


IC-FEP-VPX6b

Example of tightly coupled EW architecture

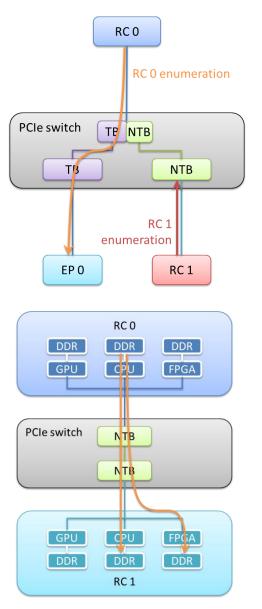
IC-INT-VPX6a







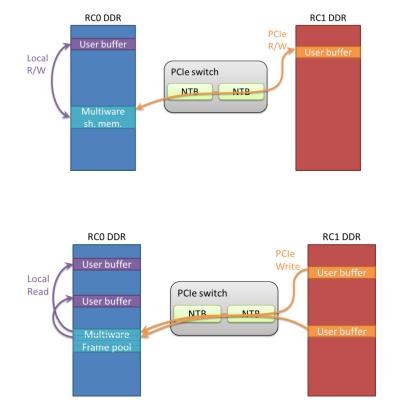
Multiware Definitions & Principles



- A PCIe domain is made of one Root Complex(RC), PCIe Transparent Bridges or switches (TB)and PCIe EndPoint (EP)
- A PCIe domain must not contain several RCs
- PCIe domains are interconnected through Non-Transparent Bridge
- NTB mechanisms for RC communication : Message boxes and Doorbells
- Use of MSI to generate interrupts on RC
- Data transfres from/to PCIe memory area (CPU DDR, Graphic DDR, FPGA DDR)
- Each RC configures its NTB access to the other PCIe domain
- Multicast : transfer same data from a PCIe memory area to several PCIe memory areas



Multiware Overview



- Software package : Configure and manage NTB hardware devices and provide simplified API for user designs
- Independent of the CPU architecture (PowerPC 32bits or 64bits Intel 32bits or 64bits)
- OS: Linux, VxWorks
- Memcpy: CPU transfers data through the NTB
- Platform DMA: Based on DMA OS API (Freescale SOC DMA, IOTA DMA...)
- NTB DMA: DMA in the PCIe switch
- Shared Memory Data Transfer
- Frame pool data transfers
- RC communication: Message transfers, events notifications, synchronization
- Information about local/remote RC
- PCIe device translation